REMARKS

The specification has been amended to correct minor grammatical errors. Claims 1, 3 and 8 have been amended. New claims 11 - 13 have been added. Claims 2 and 7 have been canceled. Claims 1, 3 - 6 and 8-13 remain pending in the application. Reexamination and reconsideration of the amended application respectfully is requested.

The Examiner rejected claim 1 under 35 USC 102(b) as being anticipated by *Hosono et al.* Claim 1 has been amended, and it is submitted that the rejection is inapplicable to the amended claim.

Referring to the reference numerals in the drawings for convenience of explanation only, the present invention as defined in amended claim 1 is directed to a semiconductor device, having at least one of a protruding electrode 2 and wiring formed on one surface of a semiconductor substrate, and a first resin film formed on the one surface, wherein the first resin film 3 has elasticity lower than 5 GPa, reducing stress induced by a difference in thermal expansion coefficient between the semiconductor substrate and the first resin film.

Hosono et al. discloses at col. 5, lines 44-48, elastomeric layer 6A and 6B composed of a synthetic resin of an elasticity that reduces thermal stress due to differences in thermal expansion coefficients between a semiconductor chip 7 and a tape carrier composed on an insulating film 1. *Hosono et al.* fail to disclose or even to suggest that a first resin film reduces stress induced by a difference in thermal expansion coefficient between a semiconductor substrate and the resin film, or that the first resin

film has elasticity lower than 5 GPa. Claim 1 therefore is neither anticipated by or obvious over the teachings of *Hosono et al*. The rejection accordingly should be withdrawn.

The Examiner also rejected claim 8 under 35 USC 102(b) as being anticipated by *Kanedo*. Claim 8 has been amended, and it is submitted that the rejection is inapplicable to the amended claim.

Claim 8 is directed to a semiconductor device having a resin film formed to cover a surface of a semiconductor chip, a post bonded to an electrode pad formed on the chip, and penetrating the resin film, and a passivation layer on the surface of the chip, between the chip and the resin film and covered by the resin film so as to have an interface therewith. A portion of the post in close proximity to a junction portion with the electrode pad is made of gold, and a portion of the gold portion faces the passivation film/resin film interface. Claim 8 reads on the embodiments of the invention illustrated in Figs. 4 and 5.

Fig. 5 of *Kaneko* discloses a projection electrode 15 made of gold that does not face an interface between the protective film 13 and the sealing resin 20. To the contrary, the common electrode film 14, which is disposed between the connection pad 12 and the gold projecting electrode 15, projects from the passivation film and faces the interface. Therefore, amended claim 8 clearly patentably distinguishes the invention over *Kaneko*, and the rejection accordingly should be withdrawn.

The Examiner rejected claim 2 under 35 USC 103(a) as being unpatentable over

Hosono et al. in view of *Shibamoto et al.* Claim 2, depending from claim 1, has been canceled.

It is also noted that *Shibamoto et al.* discloses a sealing resin layer 8 used for sealing a semiconductor chip 1 and wires 15. *Shibamoto et al.* discloses that the sealing resin 8 may have an elastic modulus of is "5-30 GPa or more, preferably 10 GPa or more, to be higher than that of the adhesive 5 gluing a stiffener 14 and a heat sink 4. To the contrary, claim 1 has been amended to specify that the first resin film has elasticity lower than 5 GPa. The claim specifies that this elasticity reduces stress induced by a difference in thermal expansion coefficient between the semiconductor substrate and the first resin film.

Thus, a person or ordinary skill in the art would not find it obvious combine the teachings of *Shibamoto et al.* and *Hosono, et al.* to obtain the claimed invention. That is, a person of ordinary skill in the art would not combine the references' teachings, and even if combined the claimed invention would not be obtained. Neither reference discloses the first resin film of the invention having an elasticity lower than 5 GPa. Moreover, *Shibamoto et al.* uses a higher elasticity material for a different purpose than the present invention and also different from the purpose of *Hosono et al.* to reduce thermal stress due to differences in thermal expansion coefficients between a semiconductor chip 7 and a tape carrier composed on an insulating film 1, as disclosed at col. 5, lines 44-48. Claim 1 is therefore clearly patentable as well over *Shibamoto et al.* and *Hosono et al.*

The Examiner also rejected claims 3 and 6 under 35 USC 103(a) as being unpatentable over *Hosono et al.* in view of *Yamaji* and Amami *et al.* The rejection respectfully is traversed.

Claim 3 has been amended merely to be in independent form, including the limitations of original claim 1. Claim 3 specifies that a second resin film having one of higher elasticity and higher strength than the first resin film is formed on the other surface of the semiconductor substrate.

Regarding claim 3, the Examiner acknowledges that *Hosono et al.* and *Yamaji* fail to disclose a second resin film formed on the other surface of the substrate having higher strength than the first resin film. The Examiner states that *Amami et al.* disclose at paragraph [0015] thermoplastic resin with low bonding strength and at paragraph [0016] thermosetting resin with high bonding strength. However, *Amami et al.* fail to disclose the above claimed feature of claim 3. That is whereas claim 3 specifies that the second resin film itself higher strength, *Amami et al.* merely discusses the bonding strength. Thus the combination of *Hosono et al.*, *Yamaji* fail and *Amami et al.* fail to disclose a second resin film formed on the other surface of the substrate having higher strength than the first resin film, and the Examiner does not even assert that the references teach a second resin film having higher elasticity. Claim 3 *therefore is deemed clearly to be patentable over Hosono et al., Yamaji* fail and *Amami et al.*, and the rejection accordingly should be withdrawn.

Regarding the rejections of claims 4 - 6, 9 and 10 over of *Hosono et al.* or

Kanedo alone or with secondary references such as *Yamaji*, *Amami et al*. *Shibamoto et al*. and/or *Lam*, the secondary references fail to show or suggest any of the feature of the invention missing from the references applied against the claims from which they depend, as discussed above. Therefore, claims 4-6, 9 and 10 are deemed clearly to be patentable for at least the reasons advance above as to the patentability of 1, 3 and 8, and the rejection accordingly should be withdrawn.

New claims 11 – 13, all directed to the elected invention, further distinguish the claimed invention over the cited references. For example, none of the cited references disclose or suggest a semiconductor device wherein a passivation layer has a thickness greater than a thickness of an electrode pad and a gold portion of a post projects below the surface of the passivation layer at a passivation film/resin film interface into confrontation or contact with the electrode pad.

Based on the above, it is submitted that the application is in condition for allowance and such a Notice, with allowed claims 1, 3 - 6 and 8 - 13, earnestly is solicited.

Respectfully submitted,

January 27, 2005
Date

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